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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,834	12/27/2001	Brett W. Murdock	1280.SC11318TH	9616

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EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,834	MURDOCK ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _05 July 2005_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-21_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _7_ is/are allowed.

6)☒ Claim(s) _1-6 and 8-21_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _15 April 2002_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ND

DETAILED ACTION

Response to Arguments

In view of applicant's remarks, filed on July 15th, 2005, the finality of the last office action is hereby withdrawn and a new grounds of rejection is presented. The rejection of claims 1-21 has been re-structured to show a clearer correspondence to the limitations presented in the current application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-10, 16, 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (2003/0005247) in view of Hahm (6,233,646).

Regarding Claims 1 and 21, Chang discloses a memory access system (Figure 2) wherein a first mode of operation, facilitating access of a portion of a first memory storage location associated with a first memory address within the 1Mbytes address range (Claim 1, "accessing first addressing range under a first operating mode..." and Page 1, paragraphs 0005 to 0008 explain standard access during real mode versus the non-standard access of accessing beyond the 1Mbyte range); and when in a second mode of operation (Claim 1, "accessed said second addressing range under a second operating mode..." and Page 2, paragraph 0033), utilizing the first output (output link from CPU 200 to memory 240) to provide an address bit of a second memory address for facilitating designation of a second memory storage location (beyond the

1Mbytes address range) of the memory. This is accomplished via a software interrupt interface which transmits a command to the CPU's system management interface hardware [SMI] thus triggering the CPU into the System Management Mode [SMM] in which mode the SMI can access the memory space whose addressing range is beyond the 1 Mbyte range. Since the SMM allows for normal access of this addressing range by the SMI, the access is completed through the use of address bits identifying the memory address to be accessed (see Page 3, paragraph 0036).

Chang does not teach using a first output coupled to the memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address.

Hahm discloses a first output (Figure 1, "enable" output from External Memory Address and Control Signal Generator 7) coupled to the memory 300 to provide a data lane enable ("enable" signal) for facilitating access (controlling read and write operation of the data, see Figure 1 and Col. 3, lines 15-16, 28-35, and Col. 4, lines 34-40) of a portion of a first memory 300 storage location associated with a first memory address ("address (19)" output from External Memory Address and Control Signal Generator 7). Although in the system of Chang, the access operation is controlled within the CPU, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller takes full control of read and write access operations (Column 3, lines 5-35) thus, allowing for the CPU to dedicate its resources to other processes.

Claim 19 is rejected using the same rationale as that of Claim 1. Additionally, Hahm discloses a processing module coupled to a set of outputs (control logic unit 1 within memory interface controller 100, Figure 1); and a memory operably coupled to the processing module (associative memory 3), wherein the memory stores operational instructions (sequence numbers) and outputs a match address causing the processing module to issue the control and enabling signals for the access of the memory 300 (Column 4, lines 10-40).

Regarding Claim 10, Chang in view of Hahm discloses the memory access system (Figures 2 and 3) further comprising:

when in the first mode of operation (accessing within the 1Mbyte addressing range, Page 1, paragraphs 0005 to 0008), utilizing a second output to provide an address bit of the first memory address for facilitating designation of the first memory storage location (Hahm, Figure 1, address(19) output from External Memory Address and Control Signal Generator 7 to Extended RAM 300 and RAM 200); and

when in the second mode of operation (accessing beyond the 1Mbyte addressing range, Page 1, paragraphs 0005 to 0008), utilizing a second output to provide a second data lane enable (command transmitted from software interrupt interface 160 to the system management interface acts as a second data lane enable since it facilitates the access into the beyond 1Mbyte addressing range by triggering the CPU to enter the System Management Mode, Page 2, paragraph 0033) for facilitating access of a portion of the second memory storage location associated with the second memory address.

Regarding Claim 16, Chang discloses a memory access system (see Figures 2 and 3) comprising:

a first register (real mode register 100 within CPU 200) having an output to indicate one of a first mode of operation and a second mode of operation (software interrupt request wherein a software interrupt request is outputted when the access requested is for an address range beyond the 1Mbyte range and thus indicates a first mode of operation);

an address control portion (software interrupt interface 160) having an input coupled to the output of the first register (Real Mode Register 100) and an output to indicate a value of an address bit when in the first mode of operation (Since the first mode of operation is described as that of accessing beyond the 1Mbyte addressing range, the software interrupt interface transmits a command to the system management interface in the CPU thus, enabling the access beyond the 1Mbyte range and using addresses for performing the access, paragraph 0036 and paragraphs 0005, 0008, and 0033).

Chang discloses a second mode of operation wherein data in memory is accessed (facilitating access of a portion of a first memory storage location associated with a first memory address) within the 1Mbytes address range (Claim 1, "accessing first addressing range under a first operating mode..." and Page 1, paragraphs 0005 to 0008 explain standard access during real mode versus the non-standard access of accessing beyond the 1Mbyte range); and an output pin from CPU (control portion) coupled to memory 240.

Chang does not teach a first data lane enable control portion for facilitating access of a portion of a first memory storage location associated with a first memory address through the output of a first data lane enable value.

Hahm discloses a first output (Figure 1, "enable" output from External Memory Address and Control Signal Generator 7) coupled to the memory 300 to provide a data lane enable

("enable" signal) for facilitating access (controlling read and write operation of the data, see Figure 1 and Col. 3, lines 15-16, 28-35, and Col. 4, lines 34-40) of a portion of a first memory 300 storage location associated with a first memory address ("address (19)" output from External Memory Address and Control Signal Generator 7).

Although in the system of Chang, the access operation is controlled within the CPU, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller takes full control of read and write access operations (Column 3, lines 5-35) thus, allowing for the CPU to dedicate its resources to other processes.

Regarding Claims 2-4, when accessing external memories the memories being accessed can be different memories (as shown in Hahm where a RAM 200 and an Extended RAM 300 can be accessed). Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, the system could be accessing these addressing ranges within independent memories, which can be of different widths (byte wide or word wide). Additionally, since a word (i.e. 16 or 32) is always bigger than a byte (which is 8 bits) it is understood that a word wide memory has more than 8 bits associated with it.

Regarding Claim 5, Chang discloses the first output being the first output of a first device (CPU 200); and the first and second modes of operation utilize the first output to access a second device (Memory 240) external to the first device (see Figure 2).

Regarding Claims 8-9, 18, Chang teaches a mode of operation being one of the first mode of operation and the second mode of operation. This system determining the mode of operation

when the system realizes which address range needs to be accessed. If the system discovers that the first address range needs to be accessed, it determines that the current mode of operation is the first mode of operation. The same goes for the scenario when the second address range needs to be accessed. This is embodied in Figure 3 (specifically for one of the modes of operation) wherein a Real Mode Register 100 invokes a Software interrupt request causing an interrupt interface to transmits a command to the system management interface, thus creating a chip select which arises the system management mode allowing for the access to occur (page 2, paragraph 0033). Additionally, the operation which requests the access to one address over another essentially performs a chip select for the addressing range to be accessed ("a specific chip select", see Page 4, claim 1).

3. Claims 6, 11-15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Hahm and further in view of Microsoft Computer Dictionary, where the Microsoft Computer Dictionary is used as an evidentiary reference.

Regarding Claims 6 and 20, Chang in view of Hahm disclose the invention as set forth by claims 5 and 19 above. Chang in view of Hahm does not teach a third mode of operation in which the system accesses internal storage (a third addressing range). Since computer systems (such as CPU 200) are known to have internal primary storage for their direct access (Main Memory, see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage.

Regarding Claim 11 Chang discloses a method of providing data to a set of pins of a device (input of memory 240), the set of pins coupled to a memory, the method comprising: during a first mode of operation (accessing the address range within the 1Mbyte range) multiplexing (transmitting a number of signals simultaneously) a first set of data onto the set of pins to access the data within the 1Mbytes address range (Claim 1, "accessing first addressing range under a first operating mode…" and Page 1, paragraphs 0005 to 0008 explain standard access during real mode versus the non-standard access of accessing beyond the 1Mbyte range); during a second mode of operation (accessing data beyond the 1Mbyte addressing range, Page 1, paragraphs 0005 to 0008), multiplexing (transmitting a number of signals simultaneously, such as signals representing accessing command) a second set of data onto the pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address (least/most significant bits of address for access, paragraph 0036), and two lane enables (software interrupt service routine and command transmitted from software interrupt interface 160 to the system management interface act as two data lane enables since they facilitates the access into the beyond 1Mbyte addressing range by triggering the CPU to enter the System Management Mode, Page 2, paragraph 0033).

Chang does not teach providing to the memory data representing two least significant bits of a first address, a most significant bit of the first address (both within address (19)), and a lane enable (enable signal outputted from external memory address and control signal generator 7).

Hahm discloses a first output (Figure 1, "enable" output from External Memory Address and Control Signal Generator 7) coupled to the memory 300 to provide a data lane enable ("enable" signal) for facilitating access (controlling read and write operation of the data, see

Figure 1 and Col. 3, lines 15-16, 28-35, and Col. 4, lines 34-40) of a portion of a first memory 300 storage location associated with a first memory address ("address (19)" output from External Memory Address and Control Signal Generator 7). Although in the system of Chang, the access operation is controlled within the CPU, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller takes full control of read and write access operations (Column 3, lines 5-35) thus, allowing for the CPU to dedicate its resources to other processes.

Chang in view of Hahm does not teach accessing a third addressing range. Since computer systems (such as CPU 200) are known to have internal primary storage for their direct access (Main Memory, see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into the system of the combination of Chang in view of Hahm the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage. Since the modified system of Chang in view of Hahm only has two modes of operation, only one lane enable is necessary for its operation. However, it is understood that in adding another mode of operation more lane enables and chip selects are needed in order to differentiate between operation modes and addressing ranges.

Regarding Claim 15, Chang discloses an apparatus (Figures 2 and 3) comprising:

a node coupled to a memory (240) to provide address data for address bit locations A(n) through A(2), where A(n) represents a most significant bit for at

least a first mode of operation (address data can represent data addressing ranges within the 1Mbyte addressing range or beyond the 1Mbyte addressing range of memory 240, Page 1, paragraphs 0005 to 0008);

a first output coupled to the memory to provide one of an address data for address bit location A(1) (address location representing addressing range within the 1Mbyte addressing range);

a second output node coupled to the memory to provide one of an address data for address bit location A(0) (address location representing addressing range beyond the 1Mbyte addressing range) .

Chang discloses a memory access system (Figure 2) wherein a first mode of operation data in memory is accessed (facilitating access of a portion of a first memory storage location associated with a first memory address) within the 1Mbytes address range (Claim 1, "accessing first addressing range under a first operating mode…" and Page 1, paragraphs 0005 to 0008 explain standard access during real mode versus the non-standard access of accessing beyond the 1Mbyte range); and when in a second mode of operation data in memory is accessed beyond the 1Mbytes address range (Claim 1, "accessed said second addressing range under a second operating mode…" and Page 2, paragraph 0033) through the use of a first output (output link from CPU 200 to memory 240) coupled to the memory to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory. This is accomplished via a software interrupt interface which transmits a command to the CPU's system management interface hardware [SMI] thus triggering the CPU into the System Management Mode [SMM] in which mode the SMI can access the memory space whose

addressing range is beyond the 1 Mbyte range. Since the SMM allows for normal access of this addressing range by the SMI, the access is accomplished through the use of address bits identifying the memory address to be accessed (see Page 3, paragraph 0036).

Chang does not teach using a first output coupled to the memory to provide a data lane enable for facilitating access of a portion of a first memory storage location associated with a memory address or a set of output pins being coupled to a memory.

Hahm discloses a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and a write signals and these outputs are directly coupled to a memory 300 (See Figure 1). In Hahm, individual output pins are represented by individual output lines. Hahm also discloses a first output (Figure 1, "enable" output from External Memory Address and Control Signal Generator 7) coupled to the memory 300 to provide a data lane enable ("enable" signal) for facilitating access (controlling read and write operation of the data, see Figure 1 and Col. 3, lines 15-16, 28-35, and Col. 4, lines 34-40) of a portion of a first memory 300 storage location associated with a first memory address ("address (19)" output from External Memory Address and Control Signal Generator 7). Although in the system of Chang, the access operation is controlled within the CPU, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang to employ the use of the memory interface controller 100 of Hahm when performing memory accesses since the memory interface controller takes full control of read and write access operations (Column 3, lines 5-35) thus, allowing for the CPU to dedicate its resources to other processes.

Chang in view of Hahm does not teach accessing a third addressing range. Since computer systems (such as CPU 200) are known to have internal primary storage for their direct access (Main Memory, see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into the system of the combination of Chang in view of Hahm the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage. Since the unmodified system of Chang only has two mode of operation, only one lane enable is necessary for it operation. However, it is understood that in adding another mode of operation more lane enables and chip selects are needed in order to differentiate between operation modes and addressing ranges. If three modes of operation are provided in the system, the three different addressing thresholds could be accessed through three different address bit locations (A(1), A(O), and A(n+1)).

Regarding Claims 12 and 13, when accessing memories, a system's memory access can be directed remote or local memories, as long as access paths are present for these memories. Since Chang teaches the accessing of "addressing ranges" which are being accessed independently in different accessing modes, the system could be accessing these addressing ranges within independent memories (as shown by Hahm where RAM 200 and RAM 300 can be accessed). In adding additional modes of operation to include the accessing of internal and external memories, the memories being accessed can be internal within the main system, or external type outside of the main system.

Regarding Claim 14, Chang teaches determining the mode of operation based upon a chip select when the system realizes which address range needs to be accessed. If the system

discovers that the first address range needs to be accessed, it determines that the first mode of operation needs to be in place. The same goes for the scenario when the second address range needs to be accessed. Additionally, the operation which requests the access to one address over another essentially performs a chip select for the addressing range to be accessed ("a specific chip select", see Page 4, claim 1). This is embodied in Figure 3 (specifically for one of the modes of operation) wherein a Real Mode Register 100 invokes a Software interrupt request, an interrupt interface transmits a command to the system management interface, thus creating a chip select which arises the system management mode which allows for the accessing to occur (page 2, paragraph 0033).

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Hahm and further in view of the Authoritative Dictionary of IEEE Standard Terms, where the IEEE Dictionary is being used as an evidentiary reference.

Chang in view of Hahm teaches the invention as set forth by claim 16 above. Chang in view of Hahm does not teach a multiplexor used to transmit a number of inputs to the address control portion while supplying one output. However, in systems where a selection is being made from two modes of operations, it is common to use a multiplexor to enable the selection (see IEEE Dictionary, Page 716). It would have been obvious to one of ordinary skill in the art at the time the invention was made use a multiplexor in the system of Chang for selection purposes since a multiplexor enables for quick signal selections (see term definition).

Allowable Subject Matter

5. Claim 7 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of Record does not teach an address bit used to extend an address range when a memory having a width less than a word is being accessed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 22nd, 2005

Midys Rojas

Midys Rojas
Examiner
Art Unit 2189

MR

Mano Padmanabhan
7/25/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER